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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,892	07/03/2003	Howard E. Rhodes	M4065.0646/P646	3670

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EXAMINER

LANDAU, MATTHEW C

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 12/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/611,892

Applicant(s)

RHODES, HOWARD E.

Examiner

Matthew Landau

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 November 2006.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,4-10,13-20,26-34,37-39 and 41-45 is/are pending in the application.
4a) Of the above claim(s) 44 is/are withdrawn from consideration.
5) ☒ Claim(s) 1,4-10,13,14 and 26-31 is/are allowed.
6) ☒ Claim(s) 15-20,32-34,37-39,41-43 and 45 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

The indicated allowability of claims 15, 32, and 38 is withdrawn in view of the newly discovered reference(s) to Sasaki. Rejections based on the newly cited reference(s) follow.

Response to Amendment

The after final amendment filed November 6, 2006 has been entered. In light of the newly discovered references listed above and the new grounds of rejection that follow, the finality of the previous office action has been withdrawn.

Election/Restrictions

Since claim 38 is no longer held to be allowable, the rejoinder presented in the Office Action mailed on July 20, 2006 is no longer valid. Therefore, claim 44 is withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on January 24, 2005.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 41 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 41 recites the limitation "said floating diffusion region". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 15 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al. (US Pat. 6,166,405, hereinafter Kuriyama) in view of Komuro (US Pat. 5,780,902) and Sasaki (US Pat. 6,521,926).

Regarding claim 15, Figure 1 of Kuriyama discloses a semiconductor substrate 10; a transfer transistor 12 (col. 5, lines 20-24) over said substrate, said transfer transistor having a single active area extension region 14b located on a first side of said transfer transistor; a photosensor 13 (col. 5, line 66 – col. 6, line 5) in electrical communication with said transfer transistor, said photosensor being within said substrate on a second side of said transfer transistor which is opposite to said first side; a reset transistor gate, and a floating diffusion region 14b on the first side of said transfer transistor and adjacent said reset transistor gate, said floating

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diffusion region in electrical communication with said active area extension region and comprising an n-type doped region at the surface of said substrate and spanning said floating diffusion region and said single active area extension region 14a. Note that the upper portions of regions 14a and 14b together can be considered the “n-type doped region”.

Kuriyama does not explicitly disclose the reset transistor gate over said substrate and spaced apart from said transfer transistor. Figure 5 of Sasaki discloses a MOS type image sensor comprising a transfer (read) transistor gate 23 and a reset transistor gate 22 over a substrate 60 and spaced apart from said transfer transistor. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including the reset transistor on the substrate for the purpose of increasing the integration density.

A further difference between Kuriyama and the claimed invention is a halo implant below said single active area extension region. Figure 5C of Komuro discloses a MOS transistor with a halo implant region 14 formed in the channel (below an LDD region). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including a halo implant region as taught by Komuro for the purpose of suppressing the short channel effect and also the hot carrier generation (see abstract of Komuro). Although Komuro refers to region 14 as a pocket implant region, it is known in the art that terms “pocket” and “halo” are synonymous.

Regarding claim 17, a further difference between Kuriyama and the claimed invention is the gate having a length which is greater than that of all other transistor gates of said pixel. Figures 4 and 5 of Sasaki disclose a MOS type image sensor comprising a transfer (read)

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transistor gate 23 having a gate length (ℓ_1) greater than all other transistors of the pixel. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Kuriyama by having the gate length of the transfer gate 12 longer than that of all other transistor gates in a pixel. The ordinary artisan would have been motivated to further modify the invention of Kuriyama in the manner described above for the purpose of suppressing the punch through current between the source and drain of the transfer (read) transistor, without unnecessarily increasing the size of the other transistors. Sasaki discloses leakage current in the read (transfer) transistor most influences the characteristics of the pixel, therefore that transistor requires the most leakage current protection (col. 10, lines 15-33 of Sasaki).

Regarding claims 18 and 19, Regarding claims 18 and 19, a further difference between Kuriyama and the claimed invention is said reset transistor comprises two active area extension regions as lightly doped drains on opposite sides of said reset transistor. Figure 5C of Komuro discloses LDD regions 5 on opposite sides of a MOS transistor. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including LDD regions on opposite sides of the reset transistor for the purpose of suppressing short channel effects and hot carrier generation, which is well known in the art. Note that a device having active area extension regions on both sides still reads on the limitation “a single active area extension region on a side opposite said floating diffusion region”, since there is a single extension region on the opposite side. In other words, the opposite side does not have more than one extension region.

Regarding claim 20, Figure 1 of Kuriyama discloses a row select transistor (select FET) and a source follower transistor (amplification FET).

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama in view of Komuro and Sasaki as applied to claim 15 above, and in further view of Choi et al. (US Pat. 5,793,088, hereinafter Choi).

Regarding claim 16, a further difference between Kuriyama and the claimed invention is a threshold voltage adjustment implant in said substrate below a gate of said transfer transistor. Figure 5 of Choi discloses a MOS transistor comprising a source/drain extension region 126, a halo implant region 120C, and a threshold voltage adjustment implant region 120A (col. 6, lines 25-28 and lines 39-49). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Kuriyama by additionally including a threshold voltage adjustment implant for the purpose of compensating for the edge effect associated with the halo implant and reducing junction capacitance (see abstract of Choi).

Claims 32-34, 37-39, 42, 43, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama in view of Komuro, Choi, and Sasaki.

Regarding claims 32, 34, and 37, Figure 1 of Kuriyama discloses a pixel array (col. 2, lines 24-26) for supplying signals to an image processor, at least one pixel of said array

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comprising: a photoconversion device 13 (photodiode)(col. 5, line 66 – col. 6, line 5); a first transistor gate (transfer transistor) 12 in electrical communication with said photoconversion device at a first side (left side) of said transistor gate; a single lightly doped drain (LDD) 14b on a second side (right side) of said transistor gate opposite said first side; and channel region under said transistor gate. It is inherent that the pixel array of Kuriyama supplies signals to some type of image processor.

A difference between Kuriyama and the claimed invention is a halo implant below said LDD. Figure 5C of Komuro discloses a MOS transistor with a halo implant region 14 formed in the channel (below an LDD region). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including a halo implant region as taught by Komuro for the purpose of suppressing the short channel effect and also the hot carrier generation (see abstract of Komuro). Although Komuro refers to region 14 as a pocket implant region, it is known in the art that terms “pocket” and “halo” are synonymous.

A further difference between Kuriyama and the claimed invention is said channel region having a threshold voltage adjustment implant. Figure 5 of Choi discloses a MOS transistor comprising a source/drain extension region 126, a halo implant region 120C, and a threshold voltage adjustment implant region 120A (col. 6, lines 25-28 and lines 39-49). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Kuriyama by additionally including a threshold voltage adjustment implant for the purpose of compensating for the edge effect associated with the halo implant and reducing junction capacitance (see abstract of Choi).

A further difference between Kuriyama and the claimed invention is the gate having a length which is greater than that of all other transistor gates of said pixel. Figures 4 and 5 of Sasaki disclose a MOS type image sensor comprising a transfer (read) transistor gate 23 having a gate length (ℓ_1) greater than all other transistors of the pixel. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Kuriyama by having the gate length of the transfer gate 12 longer than that of all other transistor gates in a pixel. The ordinary artisan would have been motivated to modify the invention of Kuriyama in the manner described above for the purpose of suppressing the punch through current between the source and drain of the transfer (read) transistor, without unnecessarily increasing the size of the other transistors. Sasaki discloses leakage current in the read (transfer) transistor most influences the characteristics of the pixel, therefore that transistor requires the most leakage current protection (col. 10, lines 15-33 of Sasaki).

Regarding claim 33, Figure 1 of Kuriyama discloses a surface n-type layer 14a over said LDD. As shown in Figure 1 of Kuriyama, a portion of region 14b extends beneath a portion of region 14a. Therefore, it can be considered region 14a is over region 14b.

Regarding claim 38, Figure 1 of Kuriyama discloses a transistor 12 in electrical contact with a photodiode 13 (col. 5, line 66 – col. 6, line 5), said transistor comprising a single active area extension region 14b on a side of said transistor opposite from said photodiode, an n-type layer 14b over said single active area extension region. As shown in Figure 1 of Kuriyama, a portion of region 14b extends beneath a portion of region 14a. Therefore, it can be considered region 14a is over region 14b. A difference between Kuriyama and the claimed invention is a halo implant below said single active area extension region. Figure 5C of Komuro discloses a

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MOS transistor with a halo implant region 14 formed in the channel (below an LDD region). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including a halo implant region as taught by Komuro for the purpose of suppressing the short channel effect and also the hot carrier generation (see abstract of Komuro). Although Komuro refers to region 14 as a pocket implant region, it is known in the art that terms “pocket” and “halo” are synonymous.

A further difference between Kuriyama and the claimed invention is a threshold voltage adjustment implant below said transistor. Figure 5 of Choi discloses a MOS transistor comprising a source/drain extension region 126, a halo implant region 120C, and a threshold voltage adjustment implant region 120A (col. 6, lines 25-28 and lines 39-49). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Kuriyama by additionally including a threshold voltage adjustment implant for the purpose of compensating for the edge effect associated with the halo implant and reducing junction capacitance (see abstract of Choi).

A further difference between Kuriyama and the claimed invention is the gate having a length which is greater than that of any other transistor gates of said pixel. Figures 4 and 5 of Sasaki disclose a MOS type image sensor comprising a transfer (read) transistor gate 23 having a gate length (ℓ_1) greater than all other transistors of the pixel. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Kuriyama by having the gate length of the transfer gate 12 longer than that of all other transistor gates in a pixel. The ordinary artisan would have been motivated to modify the invention of Kuriyama in the manner described above for the purpose of suppressing the punch

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through current between the source and drain of the transfer (read) transistor, without unnecessarily increasing the size of the other transistors. Sasaki discloses leakage current in the read (transfer) transistor most influences the characteristics of the pixel, therefore that transistor requires the most leakage current protection (col. 10, lines 15-33 of Sasaki).

Regarding claim 39, Figure 1 of Kuriyama discloses a floating diffusion region 14a adjacent a gate of said transistor, said single active area extension region and said halo implant adjacent at least part of said floating diffusion region (after the above combination). Note that region 14a is considered to be both the n-type layer and the floating diffusion region, since the claims do not specify that these two must be separate and distinct regions. "Floating diffusion region" can simply be a more narrow description of the n-type layer.

Regarding claim 42, it would have been further obvious to include the insulating layer 81 of Sasaki (Figure 5) (which extends over the transistor 23, photodiode D1, and floating diffusion region 64) in the device of Kuriyama for the purpose of protecting and insulating the components of the image sensor.

Regarding claim 43, the disclosure of Kuriyama does not explicitly disclose the image sensor is a CMOS imager. However, it would have been obvious to the ordinary artisan at the time the invention was made to use a CMOS imager as disclosed in the background of Kuriyama (col. 1, lines 18-25) for the purpose of integrating input elements with peripheral circuits on one chip.

Regarding claim 45, Figure 1 of Kuriyama discloses said transistor (charge transfer transistor) (col. 5, lines 20-24) is part of a pixel having at least two other transistors (reset and select transistors) in electrical communication with said photodiode 13.

Allowable Subject Matter

Claims 1, 4-10, 13, 14, 26-31 are allowed.

Regarding claims 1 and 26, the reasons for allowance were given in the Office Action mailed on February 15, 2006.

Claim 41 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record, either singularly or in combination, does not disclose or suggest the combination of limitations including said active area extension region and said floating diffusion region are laterally spaced away from a gate of said transistor by a portion of a substrate supporting said transistor.

Response to Arguments

Applicant's arguments with respect to the currently rejected claims have been considered but are moot in view of the new ground(s) of rejection.

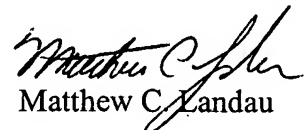
Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent 6,521,926 discloses an image sensor comprising a transfer transistor gate with a gate length greater than all other gates in the pixel (Figure 9).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Matthew C. Landau

December 1, 2006